REMARKS

1. Applicants submit this replacement amendment, which is filed to place the application in condition for allowance and to simplify issues for any appeal. Please replace the response filed on 8/25/2008 with this response.

2. The disclosure is objected to because the listing of the figures on page 7 should come before the Disclosure of the Invention. A substitute specification is submitted herein.

Support for the specification amendments is in the originally filed application. No new matter has been added.

a) Throughout the specification the term "regenerate" has been amended to be "recover" for clarity and support is found at least in on page 5 lines 1-2, "the capacitor 1 is recharged" and in claim 2 as originally filed.

b) A "SUMMARY OF INVENTION" paragraph has been added and finds support in the claims. The paragraph "BRIEF DESCRIPTION OF THE DRAWINGS" has been moved to be before the DETAILED DESCRIPTION.

c) The text and table below has been added for clarity and finds support in claim 1 as originally filed which recites in part: "the control circuit controls pairs of the four inverse-conductive semiconductor switches composing the bridge circuit positioned on diagonal lines, respectively, so that the pairs are turned on simultaneously or alternately, and controls the pairs so that when at least one of the paired two inverse-conductive semiconductor switches is on, the other paired inverse-conductive semiconductor switches are off".

"The table below indicates the ON/OFF states of the pair of switches S1 and S2 and the pair of switches S3 and S4.

	Pair		Pair		
Pattern	S1	S2	S3	S4	Remarks
1	**ON**	**ON**	OFF	OFF	When one pair is simultaneously ON, another pair is OFF.
	OFF	OFF	**ON**	**ON**	
2	**ON**	OFF	OFF	OFF	When one switch of one pair (S1, S2) is alternatively ON,
	OFF	**ON**	OFF	OFF	another pair (S3, S4) is always OFF.
3	OFF	OFF	**ON**	OFF	When one switch of one pair (S3, S4) is alternatively ON,
	OFF	OFF	OFF	**ON**	another pair (S1, S2) is always OFF.

"

3. Claims 1 line 7 "its" is objected to and line 15 is objected to as not clear. Claim 2 was objected to because there is no indication in the claim of what component is replenished (lines 4-5).

Appropriate claim amendments have been made.

4. Claims 1-3 and 5 stand rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,751,121 to Toyama.

Applicants respectfully submit that Toyama does not anticipate the present invention.

The capacitor 17 of Toyama is a smoothing capacitor which according to Toyama col. 2, lines 63-67 is provided in Toyama "to smooth alternating current voltages". This is contrary to Claim 1 which recites in part: "*an energy source capacitor initially charged is connected to a DC terminal of the bridge circuit*". In order for Toyama to anticipate Claim 1, smoothing capacitor 17 would have to be connected to a DC terminal of the

bridge circuit; however, Toyama teaches away from connecting to a DC terminal and teaches instead that smoothing capacitor 17 connected to alternating current (AC).

Further, as described in Toyama col. 3, lines 15-21, Toyama teaches that "control signals from the bridge control circuit 7… turn on and off one pair of the transistors 23a,23b and the other pair of the transistors 23c, 23d, alternately". Thus, Toyama teaches that pair 23a,23b are both ON or OFF, and that at alternate times pair 23c,23d are both ON or OFF. In Toyama one transistor of a pair is never ON while another transistor of the pair is OFF. Toyama teaches that both transistors in the pair are either ON or OFF.

Thus, Toyama does not teach claim 1, which recites in part: "a control circuit for controlling the first and second pairs of the inverse-conductive semiconductor switches positioned diagonally on the bridge circuit so that when *the two inverse-conductive semiconductor switches in the first pair are controlled to turn on simultaneously or alternately, the control circuit controls the two inverse-conductive semiconductor switches in the second pair to be off*, and so that when the *two inverse-conductive semiconductor switches in the second pair are controlled to turn on simultaneously or alternately, the control circuit controls the two inverse-conductive semiconductor switches in the first pair to be off*". Thus, in claim 1 the two inverse-conductive semiconductor switches in a pair are controlled to turn on simultaneously or alternately. This is not taught by Toyama and in fact Toyama teaches away from claim 1.

Thus, claim 1 and claims 2-7 which depend on claim 1 are not anticipated by Toyama.

5. Claims 1-7 stand rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,760,234 to Yuzurihara.

First, applicant respectfully submits that under the Hilmer doctrine that Yuzurihara is not prior art. The foreign priority date for the present application Serial No. 10/524893 is August 19, 2002. The U.S. filing date for U.S. Patent No. 6,760,234 to Yuzurihara is

August 27, 2002, which is after the priority date for the present application. The foreign application priority relates to Japan application No. 2002-197478 filed July 5, 2002; however, per MPEP 706.02(f)(1), the section 102(e) date of Yuzurihara is the U.S. filing date, which is August 27, 2002, which is after the priority date of the present application. Thus, Yuzurihara is not prior art to the present application under the Hilmer doctrine.

Also in addition to not being prior art under the Hilmer doctrine, applicants respectfully submit that regardless of the Hilmer doctrine Yuzurihara does not anticipate the present invention.

As described in Yuzurihara col. 7, lines 14-20, Yuzurihara teaches that "In the inverter 13, two pairs of the semiconductor switches facing each other, that is, a pair of the semiconductor switches Q1 and Q4 and a pair of the semiconductor switches Q2 and Q3 repeat the ON/OFF operation alternately" so that pair Q1 and Q4 are ON and then OFF and then pair Q2 and Q3 are ON and then OFF. Thus each switch in a pair is either ON or OFF. In col. 8, lines 65-67 Yuzurihara teaches that " a pair of the semiconductor switches Q1 and Q4 and a pair of the semiconductor switches Q2 and Q3 are alternately ON". In col. 9, lines 31-33 Yuzurihara teaches that "Because both of the semiconductor switches Q2 and Q3 are OFF" and in col. 9, lines 51-51 Yuzurihara teaches that "the semiconductor switches Q1 and Q4 are OFF".

Thus, Yuzurihara does not teach claim 1, which recites in part: "a control circuit for controlling the first and second pairs of the inverse-conductive semiconductor switches positioned diagonally on the bridge circuit so that when *the two inverse-conductive semiconductor switches in the first pair are controlled to turn on simultaneously or alternately, the control circuit controls the two inverse-conductive semiconductor switches in the second pair to be off*, and so that when the *two inverse-conductive semiconductor switches in the second pair are controlled to turn on simultaneously or alternately, the control circuit controls the two inverse-conductive semiconductor*

switches in the first pair to be off". Thus, in claim 1 the two inverse-conductive semiconductor switches in a pair are controlled to turn on simultaneously or alternately. This is not taught by Yuzurihara and in fact Yuzurihara teaches away from claim 1 by always turning ON each switch in a pair.

Thus, claim 1 and claims 2-7 which depend on claim 1 are not anticipated by Yuzurihara.

5. Claims 1-7 stand rejected under 35 U.S.C. 103(a) as being obvious in view of U.S. Patent No. 5,926,381 to Moriguchi.

Applicants respectfully submit that claims 1-7 are not made obvious by Moriguchi.

Moriguchi is concerned with and relates to a DC power supply apparatus that includes an input-side rectifier 4 which rectifies an input AC voltage and supplies the rectified voltage (DC) to a voltage boosting converter 6. Thus, Moriguchi is not concerned with supplying a bipolar pulse current to an inductive load connected to an AC terminal of a bridge circuit, as recited in claim 1 of the present invention. As described in Moriguchi col. 3, lines 40-43, capacitor 16 of Moriguchi is a smoothing capacitor and a DC voltage develops across capacitor 16. In Moriguchi it is not taught that capacitor 16 charges and discharges.

The four semiconductor switching devices (28 and 30, and 40 and 42) of Moriguchi correspond respectively to the inverse-conductive semiconductor switches (S4, S2, S1, S3) of the bridge circuit of the present invention. This is evident in FIG. 1 of Moriguchi in which it is shown that the positive side of capacitor 16 is connected to semiconductor switching devices 28 and 40, while in the present invention in FIG. 4 the energy sourcing capacitor positive side is connected to inverse-conductive semiconductor switches S4 and S1. Also in FIG. 1 of Moriguchi it is shown that the negative side of capacitor 16 is connected to semiconductor switching devices 30 and 42, while in the present invention

in FIG. 4 the energy sourcing capacitor negative side is connected to inverse-conductive semiconductor switches S2 and S3.

Thus in Moriguchi, semiconductor switching devices 40 and 30 are a first pair of switches and semiconductor switching devices 42 and 28 are a second pair of switches positioned diagonally on the bridge circuit.

As shown in Figs.2(a) and 2(b), Moriguchi teaches that there is a period that both semiconductor switching device 30 in the first pair and semiconductor switching device 42 in the second pair are simultaneously ON. Also, as shown in Figs.2(a) and 2(b), Moriguchi teaches that there is a period that both semiconductor switching device 40 in the first pair and semiconductor switching device 28 in the second pair are simultaneously ON.

Thus Moriguchi teaches away from claim 1 which recites in part: ""a control circuit for controlling the first and second pairs of the inverse-conductive semiconductor switches positioned diagonally on the bridge circuit so that when *the two inverse-conductive semiconductor switches in the first pair are controlled to turn on simultaneously or alternately, the control circuit controls the two inverse-conductive semiconductor switches in the second pair to be off*, and so that when the *two inverse-conductive semiconductor switches in the second pair are controlled to turn on simultaneously or alternately, the control circuit controls the two inverse-conductive semiconductor switches in the first pair to be off*". Thus, per claim 1, when either switch in the first pair is ON, then both switches in the second pair are OFF. Also, per claim 1, when either switch in the second pair is ON, then both switches in the first pair are OFF.

Thus, claims 1-7 are not made obvious in view of Moriguchi.

6. Claims 4 and 6-7 stand rejected under 35 U.S.C. 103(a) as being obvious in view of U.S. Patent No. 5,751,121 to Toyama.

Claims 4 and 6-7 dependent on claim 1. "If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious." *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). Therefore, in light of the above discussion of claim 1, Applicants submit that claims 4 and 6-7 are also allowable at least by virtue of their dependency on claim 1 as well as the additional limitations recited by each of these claims.

In view of the above, Applicants submit that the application is now in condition for allowance and respectfully urge the Examiner to pass this case to issue.

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The Commissioner is authorized to charge any additional fees which may be required or credit overpayment to deposit account no. 12-0415. In particular, if this response is not timely filed, the Commissioner is authorized to treat this response as including a petition to extend the time period pursuant to 37 CFR 1.136(a) requesting an extension of time of the number of months necessary to make this response timely filed and the petition fee due in connection therewith may be charged to deposit account no. 12-0415.

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